PATENT ABSTRACTS OF JAPAN

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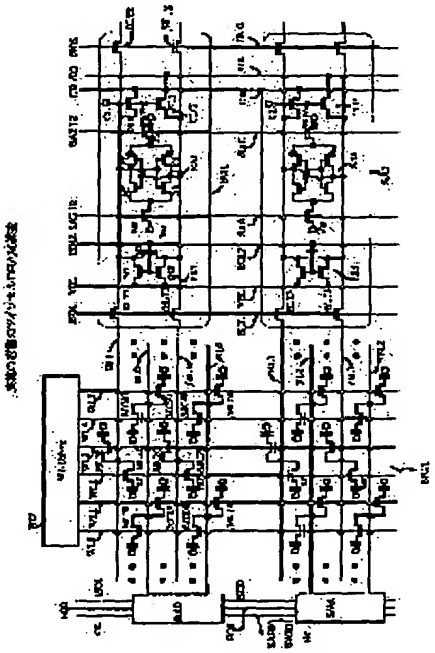
(54) DRAM FOR STORING DATA IN A PAIR OF CELLS

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a DRAM in a novel configuration, with which power consumption is reduced or operation is accelerated.
SOLUTION: Data to be stored are stored in a pair of memory cells by complementary data and a pair of these memory cells are connected to a pair of bit lines BL and /BL connected to a common sense amplifier SA in response to the selection of a word line WL. Since H and L levels are stored in a pair of memory cells corresponding to the store data of one bit, read out sensitivity is improved and a refresh cycle can be prolonged. Furthermore, the sense amplifier of a first bit line couple is arranged on one side of a cell array and the sense amplifier of a second bit line couple is arranged on the other side of the cell array. Corresponding to the word line to be selected, the sense amplifier connected to any one bit line couple is activated, the sense amplifier connected to the other bit line couple is maintained in an inactive state, and the other bit line couple is maintained at a precharge level.



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